K.K.Wagh Institute of Engineering Education and Research

Hirabai Haridas Vidyanagari, Mumbai Agra Road Amrutdham, Panchavati, Nashik, Maharashtra 422003

Minutes of Alumni Interaction

28th Aug 2020 / 10:30 AM / GoToWebinar App

ATTENDEES :

- Mr. Aniket Narkhede (Guest)
- Proff. Dr. D. M. Chandwadkar (HoD)
- Proff. Dr. Sunita Patil (Ugale)
- Staff of E&TC
- Students of E&TC

AGENDA :

- To introduce students with **VLSI Design**
- To guide students how to prepare for landing a job in VLSI domain

The following points were discussed:

- Power of transistors
- Moore's law
- Animation showing what goes on under the hood of the systems
- What is VLSI(Very Large Scale Integration)
- Design flow of VLSI IC Circuits
- VLSI architecture design and its applications
- RTL(Register Transfer Level) Design
- What is design verification test plan in VLSI
- **Processes:** Synthesis, DFT (Design for Testability), Signoff, Fabrication& Packaging
- What is SoC (System on Chip)
- Co-Processors, Memories & on-chip bus
- Future scope of VLSI in India
- Key skills required to be a good Verification Engineer